

# HA-5101

## SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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### **Introduction**

This application note describes the SPICE macro-model for the HA-5101, a low noise, high performance op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC parameters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

### **Model Description**

#### **Input Stage**

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is modeled with FA. Source VIO represents the input offset voltage. C1 limits slew rate. No input parasitics due to package capacitance and lead inductance are included.

#### **Gain Stage**

G2, R2, CC, GOL, and RD simulate open loop gain. CC is the macro-model dominant pole capacitor.

#### **Poles and Zeros**

The HA-5101 macro-model uses a complex zero modeled with RLC networks as well as five poles and three zeros. General poles use RC networks and zeros use RL networks. Singularity frequencies are indicated on the schematic.

#### **Output Stage**

EX1, D1 and D2 model output current limiting. IH and IL model the power supply currents. FIP and FIN vary the supply currents based on the op amps output current. DL, DH, VH and VL provide voltage clamping on the output to simulate the typical output voltage swing. No output parasitics due to package capacitance and lead inductance are included.

### **Parameters Not Modeled**

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

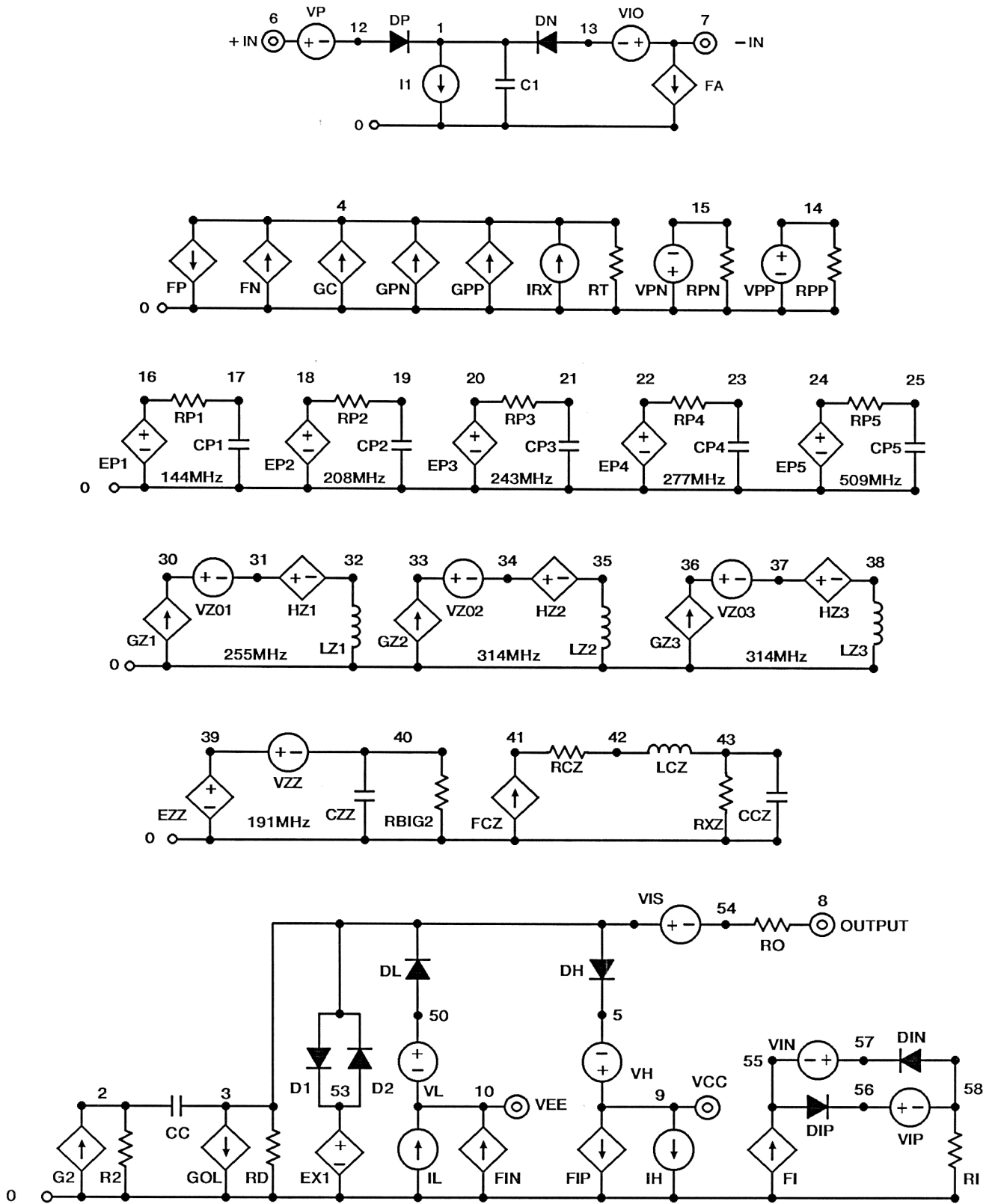
**Spice Listing**

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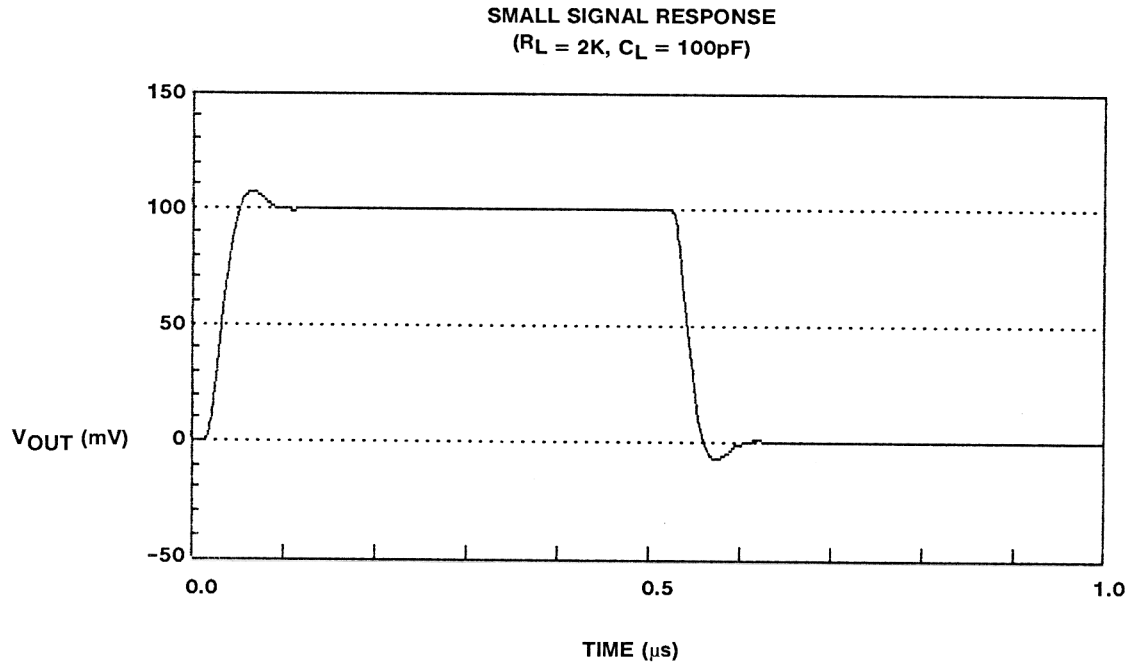
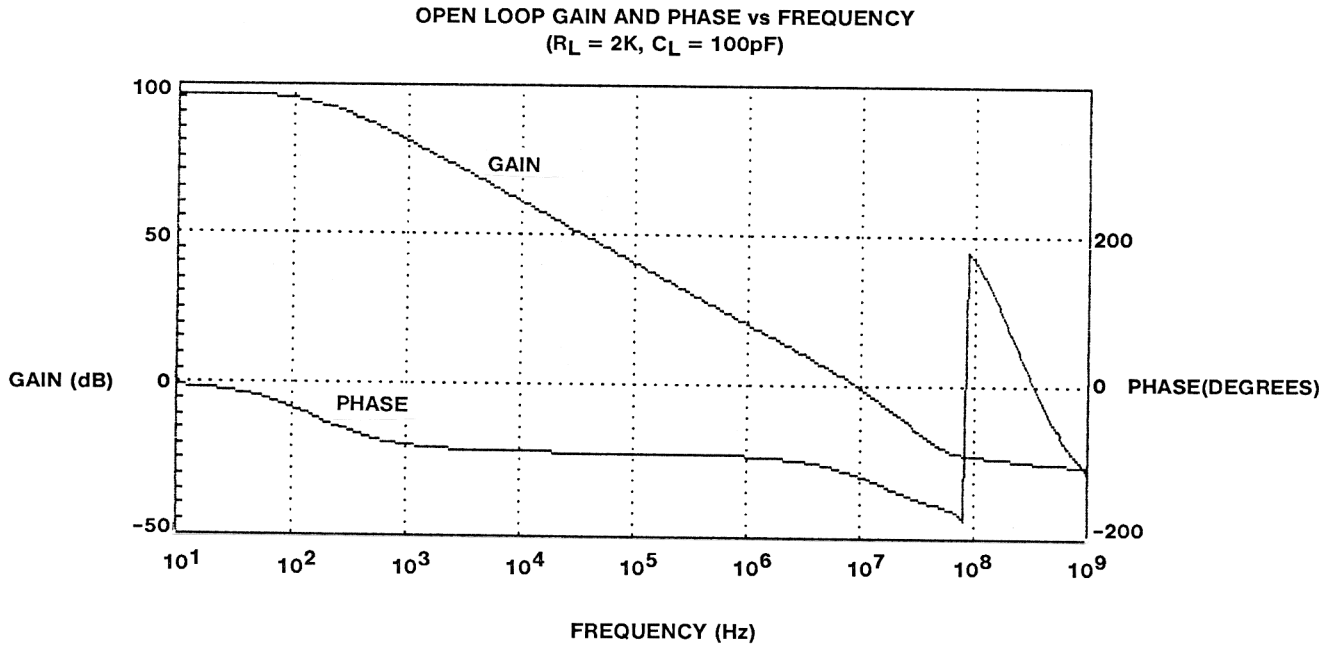
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*
*HA-5101 MACRO-MODEL
*REV. 8-8-91
*BY: D.L. YOUNGBLOOD
*
* PINOUT: +IN -IN VCC VEE OUT
*
.SUBCKT HA5101 6 7 9 10 8
.MODEL DP D IS=1E-14 N=+2.8162E+00
.MODEL DN D IS=+8.9762E-15 N=+2.8162E+00
.MODEL DV D IS=+3.0966E-14 N=.2
.MODEL D1 D IS=1E-14 N=1
.MODEL D2 D IS=1E-14 N=+1.0841E+00
*
*INPUT STAGE
*
VP 6 12 0
DP 12 1 DP
*
*THE VALUE OF SOURCE "VIO" REPRESENTS OFFSET
*VOLTAGE AND MAY BE CHANGED TO SIMULATE
*WORST CASE IF DESIRED
*
VIO 7 13 +1.5987E-04
*
DN 13 1 DN
FA 7 0 VIO +3.5294E-01
I1 1 0 +1.6130E-07
C1 1 0 +8.8812E-16 IC=-1.1545E+00
FP 4 0 VP +1.4025E+03
FN 0 4 VIO +1.5625E+03
GPP 0 4 9 14 +8.0498E-10
GPN 0 4 15 10 +3.8511E-09
RT 4 0 1.0
VPP 14 0 +1.50E+01
RPP 14 0 1K
VFN 0 15 +1.50E+01
RPN 0 15 1K
GC 0 4 1 0 +1.6475E-08
IRX 0 4 -2.667E-08
*
*GENERAL POLES
*
EP1 16 0 4 0 1.0
RP1 16 17 +9.0176E+01
CP1 17 0 1.0E-10
EP2 18 0 17 0 1.0
RP2 18 19 +1.2731E+01
CP2 19 0 1.0E-10
EP3 20 0 19 0 1.0
RP3 20 21 +1.2731E+01
CP3 21 0 1.0E-10
EP4 22 0 21 0 1.0
RP4 22 23 +1.1385E+01
CP4 23 0 1.0E-10
EP5 24 0 23 0 1.0
RP5 24 25 +6.4181E+00
CP5 25 0 1.0E-10
*
*GENERAL ZEROS
*
GZ1 0 30 25 0 +2.7671E-03
VZ01 30 31 0.0
HZ1 31 32 VZ01 +3.6139E+02
LZ1 32 0 1.0E-6
GZ2 0 33 30 0 -1.0055E-03
VZ02 33 34 0.0
HZ2 34 35 VZ02 -9.9455E+02
LZ2 35 0 1.0E-6
GZ3 0 36 33 0 -6.9434E-04
VZ03 36 37 0.0
HZ3 37 38 VZ03 -1.4402E+03
LZ3 38 0 1.0E-6
*
*COMPLEX ZERO
*
EZZ 39 0 36 0 1.0
VZZ 39 40 0.0
CZZ 40 0 1.0E-12
RZZ 40 0 1.0E+7
FCZ 0 41 VZZ 1.0
RCZ 41 42 +3.8073E+03
LCZ 42 43 +7.0771E-06
CCZ 43 0 1.0E-12
RXZ 43 0 1.0E+7
*
*GAIN/OUTPUT STAGE
*
G2 0 2 41 0 1.0
R2 2 0 +2.7509E+06
CC 2 3 +2.20E-11
GOL 3 0 2 0 +3.9807E-2
RD 3 0 +5.9935E+02
DH 3 5 DV
DL 50 3 DV
VH 9 5 -1.187E+00
VL 50 10 +1.333E+00
IH 9 0 +3.50E-03
IL 0 10 +3.50E-03
D1 3 53 D1
D2 53 3 D2
EX1 53 0 POLY 2 3 0 3 8 0 1 -2.7887E-01
RO 54 8 +4.2754E+01
VIS 3 54 0
FI 0 55 VIS 1
DIP 55 56 DV
DIN 58 57 DV
VIP 56 58 0
VIN 57 55 0
RI 58 0 1
FIP 9 0 VIP 1
FIN 0 10 VIN 1
.ENDS HA5101

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Macro-Model Schematic

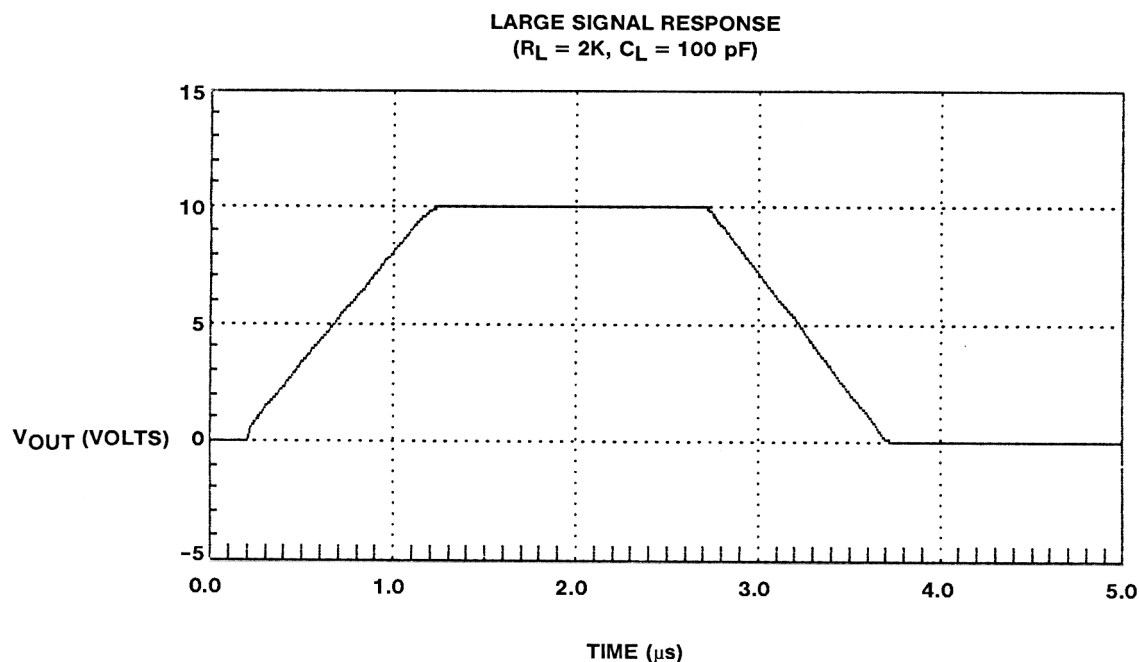


**Model Performance** Conditions:  $V_{SUPPLY} = \pm 15V$ ,  $A_{VCL} = +1$ , Unless Otherwise Specified



## Model Performance (Continued)

Conditions  $V_{SUPPLY} = \pm 15V$ ,  $A_{VCL} = +1$ , Unless Otherwise Specified



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